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The fabrication of double-gate metallic field emitter arrays with large collimation gate apertures and their field emission beam characteristics are reported. The device fabrication steps, including the molding technique for array fabrication, the electron extraction gate fabrication by the self-aligned resist etch-back method, and the fabrication of the collimation gate electrode using a focused ion beam assisted method are described in detail. The experimental results of 2×2 tip arrays with the proposed double-gate structure demonstrate an order of magnitude enhancement in beam brightness with minimal current loss. A similarly high beam brightness enhancement was achieved with a 20×20 tip array device, showing the scalability of the proposed structure. The observation of improved current-voltage characteristics with the 20×20 tip array is ascribed to the difference in gate aperture shape. The possibility of further improving the beam characteristics of double-gate field emitter arrays and the reduction of the transverse electron velocity spread are discussed. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4764925]

I. INTRODUCTION

Research on field emitter arrays (FEAs) has been actively pursued[1–13] with the aim of realizing high current and high current density cathodes, e.g., for compact microwave vacuum electronic amplifiers, such as traveling wave tubes (TWTs)[14–17] and compact free electron lasers.[7,18] FEAs are expected to help simplify the gun design and extend the operation range of such TWTs.[1,15] A recent report on a 5 GHz TWT using a single-gate Spindt FEA with 100 W output[17] demonstrates the practical feasibility of FEA-based TWTs. The possibility to generate high currents with densities above 10–100 A cm^{-2} (Ref. 19) is even more attractive for sub-millimeter and THz vacuum electronic power amplifiers.[20–22]

To take full advantage of FEAs, however, it is crucial to reduce the beam divergence of individual field emission beamlets. In a single-gate FEA, the beam divergence is in the order of 20°–30°. More than a factor of 10 reduction of this divergence could significantly simplify the gun design to inject electrons into micro-machined waveguides for THz devices.[8,9] In addition, FEAs with a normalized transverse emittance below 0.1 mm mrad for a 1 mm diameter FEA and emission current densities of ~1 kA cm^{-2} have a potential to improve the stability and performance of X-ray free-electron lasers significantly.[3,7] Such FEAs are also promising as cathodes for massively parallel electron beam lithography tools.[23]

To reduce the beam divergence and the transverse electron velocity spread, double-gate FEAs equipped with a beam collimation gate electrode G_{col} in addition to the electron extraction gate electrode G_{ext} have been intensely studied.[5,7–9,24–31] This is due to the fact that the emittance of a FEA can be small only when the individual beamlets are maximally collimated,[1] even though the emittance of individual beamlets is small.[33]

In double-gate FEAs, a divergent field emission beam is collimated by applying a negative collimation potential V_{col} to G_{col}. However, since the negative V_{col} reduces the electric field F_{tip} at the emitter tip apexes, the emission current is diminished and a part of the electrons is reflected by the negative G_{col} potential and intercepted by G_{ext}. The main challenge has been lying in minimizing the emission current reduction at the maximum beam brightness.[8,9,26–32]

We have recently shown that stacked double-gate structures with large G_{col} apertures of approximately 3 times the diameter of the G_{ext} apertures improved the emission current characteristics.[9] To fabricate these double-gate FEAs, we have developed a method using focused ion beam (FIB) milling. With this flexible and mask-less method, we realized 2×2 tip double-gate FEAs that exhibited a current density enhancement of a factor of 13.9 ± 1.0 (Ref. 9). The FIB also enables precise alignment of the G_{col} apertures to the underlying G_{ext} apertures and the emitter tips. This is a difficult task with the normally used polymer etch-back method.[5,8,9]

The aims of the present work are to report the fabrication method of our double-gate FEAs in detail, including the FIB assisted G_{col} patterning method and experimentally clarify the impact of the G_{col} aperture diameter on the collimation characteristics. Also, the scalability of the proposed large G_{col} aperture structure is investigated by applying the FIB assisted method to fabricate a 20×20 FEA and test its beam characteristics.

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II. FOCUSED ION BEAM ASSISTED FABRICATION OF DOUBLE-GATE FEAS

In this section, we describe the fabrication procedure of three double-gate FEAs, two 2×2 double-gate FEAs (FEA1 and FEA2), and one 20×20 double-gate FEA (FEA3) in detail. FEA1 and FEA2 both have G_{ext} apertures with a diameter equal to $\sim 2.0\ \mu$m. Their G_{col} aperture diameters measure $\sim 6.0\ \mu$m for FEA1 [Fig. 4(a)] and $\sim 2.3\ \mu$m for FEA2 [Fig. 4(b)]. The diameter of the G_{ext} and G_{col} apertures of FEA3 [Fig. 4(c)] are nominally the same as FEA1. In Secs. II A and II B, the fabrication procedure of metallic FEAs and the G_{ext} formation procedure that precedes the fabrication of G_{col} are described. In Sec. II C, we detail the FIB assisted method to fabricate G_{col}. Although there are optical and electron-beam lithography tools available for our required precision to fabricate devices with more than tens of thousands of emitters, these require the development of an overlay alignment method that should be adjusted for our specific purposes and device sizes. In contrast, the FIB process described hereafter allows rapid proto-typing of FEAs with different aperture sizes (such as FEA1 and FEA2) without significantly modifying the process conditions. Its high flexibility makes the FIB an ideal tool for exploring the correlation between the gate aperture sizes and the electron beam collimation characteristics.

A. Fabrication of metallic FEAs

The double-gate FEA fabrication starts with the preparation of emitter arrays supported on metallic substrates. The gate electrodes are fabricated on top of the array by the method described in Secs. II B and II C. To fabricate the metallic emitter arrays, the molding technique originally proposed by Gray and Greene[34] is used. The first step is the patterning of pyramidal pits on a 4 in. Si (100) wafer by anisotropic wet-etching [Fig. 1(a)]. As etching mask, we use a 100 nm thick thermal oxide layer, which is patterned with 1.5 μm square hole arrays aligned with a pitch of 5 or 10 μm. The final size and shape of the emitters are the same for both array pitches. To fabricate double-gate FEAs with $\sim 6\ \mu$m diameter G_{col} apertures, we used the 10 μm pitch arrays. The oxide patterning is done by photolithography and dry-etching in CHF_3 plasma using a reactive-ion etcher (RIE, Oxford RIE 100). The subsequent pit etching is done in a 20% potassium hydroxide (KOH) solution heated to 70 °C. Utilizing the slow etching rate of (111) facets, pyramidal pits are thereby formed in the Si substrate.

The sharpness of the bottom of the pits will determine the sharpness of the emitter tips in the end (see below). After the KOH etching, the obtained pit apex sharpness is typically in the order of 50–100 nm and not sufficiently small. To ultimately obtain emitter tips with apex radii of curvature of ~ 5 nm (leading to a field enhancement factor of ~ 40 (Ref. 6)), we add two oxidation steps to sharpen the pits. The first additional oxidation is done after removing the first SiO_2 layer used as KOH etching mask. At this step, the pit apexes are sharpened down to a few nanometers. This is a consequence of the stress dependent diffusion of O_2 during the thermal oxidation.[35,36] This second oxidation also sharpens the side joints of the (111) facets and introduces spikes at the topmost edge of the pits. The sharp facet joints are unfavorable since they may cause parasitic emission bombardment of G_{ext}. The spikes should be eliminated since they introduce complications in the gate fabrication process described below by causing concave edges at the bottom of the emitters. Adding a third oxidation step circumvents these problems.[4] By adjusting the thicknesses of the second and the third oxide layers, we control the final sharpness of the emitter tip apexes. Typically, we choose the second oxidation thickness to be 200 nm, and the third oxidation thickness to be 600 nm. With this combination, we obtain emitters with ~ 5 nm tip apex radii of curvature as shown in Fig. 1(b) and the inset in Fig. 4(a). The oxide thicknesses were calibrated before each fabrication run to achieve the nominal apex sharpness.

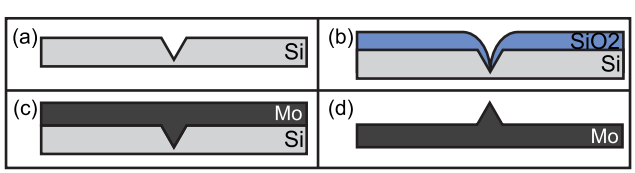

FIG. 1. Process steps used to fabricate the molybdenum field emitter arrays by the molding method. (a) Anisotropic wet-etching of the Si substrate to form pyramidal pits as molds for the emitters. (b) Thermal oxidation of the Si mold substrate is used to tailor the pit shapes and the tip apex sharpness. (c) Metallization of the mold wafer with a 1 μm thick sputtered molybdenum film (the SiO_2 layer is not shown here). (d) A molybdenum field emitter after removing the Si mold substrate.

In the next step, the mold substrate is metalized with a 1 μm thick molybdenum film that will serve as the electron emitting material [Fig. 1(c)]. This is done by magnetron sputtering using high purity Ar gas in a sputter deposition tool (Nordiko). The pressure and the flow rate of the Ar gas were adjusted to minimize the stress of the Mo film. Sputtering allows for a relatively uniform metalization of the mold pits at room temperature. The base pressure of the sputtering tool is 2×10^{-6} mbar, leading to the incorporation of about 10% O_2 into the film. This was confirmed by X-ray photoelectron spectroscopy. Nevertheless, using Ar gas with $\geq$99.999% purity, we were able to lower the room temperature resistivity of the molybdenum film to $\sim 10\ \mu\Omega$ cm, which is only twice the value of pure bulk molybdenum. High resolution scanning electron microscopy (SEM) and x-ray diffraction revealed that the molybdenum film is (110) oriented and consists of ~ 50 nm wide grain columns oriented perpendicular to the surface of the pits. The development of these grains during the deposition introduces a surface corrugation that partially blocks the Mo flux from reaching the bottom of the pits. Consequently, an empty cavity with a width in the order of tens of nm is formed beneath the emitter tip apex. These cavities are visible in the FIB cross-sections shown in Fig. 9.

On the sputtered Mo, a 100 nm thick Cr adhesion layer and a 200 nm thick Pd seed layer are deposited by electron-beam evaporation. A 400 μm thick Ni layer electro-plated on top serves as substrate of the FEA with negligible series resistance ($<10^{-3}\ \Omega$ cm). After the Ni electro-plating, the silicon substrate is completely removed by chemical etching in a heated KOH solution with the same condition as the mold pits etching. The third oxidation layer on the mold protects the emitter surface during the etching. At the end, we obtain arrays of pyramidal shaped molybdenum emitters with a base length of approximately 2 μm. Before the fabrication of

the gate electrodes, we dice the FEA wafers into 22×22 mm chips using a diamond blade saw. All further process steps are carried out on these chips.

B. Fabrication of the electron extraction gate electrode

The fabrication of the electron extraction gate electrode G_{ext} starts with the removal of the SiO_2 layer covering the molybdenum FEAs by chemical etching using a buffered oxide etch solution (BOE 7:1; NH_4F and HF in water). A 1.2 μm thick SiO_2 layer (I_1) is then deposited by plasma enhanced chemical vapor deposition (PECVD, Oxford PlasmaLab System 80). On top of this, a 500 nm thick Mo layer is sputter-deposited (G_{ext}) with the same condition as for the mold metallization. The schematic cross-section of the resulting structure is shown in Fig. 2(a).

After the deposition of the I_1 and G_{ext} layers, the chip surface exhibits ~500 nm tall protrusions on top of the emitters [Fig. 2(a)]. Utilizing these protrusions, we pattern the G_{ext} apertures by using a polymer mask and wet-etching. The etching mask is prepared by a self-aligned etch-back process: A positive photo-resist (PR, Microposit S1828) is spin-coated on top of G_{ext} and soft-baked, resulting in a planarized layer with an average thickness of ~4 μm [Fig. 2(b)]. When submitting the PR-coated FEA chip to low power oxygen plasma, the PR is uniformly thinned, and G_{ext} areas on top of the emitters are selectively exposed [Fig. 2(c)]. By adjusting the time and power of the oxygen plasma etching, the area laid bare on top of the emitters can be controlled between approximately 1.8 μm and 2.5 μm in diameter. Using the patterned PR as etching mask, we etch the G_{ext} apertures using an acid solution (H_3PO_4, CH_3CO_2H, and HNO_3 in 20% water) [Fig. 2(d)]. Afterwards, G_{ext} is further patterned into its final shape [Fig. 4(d)]. In completed double-gate FEAs, the G_{ext} electrodes are buried underneath the G_{col} electrodes with the exception of the contact pads for wire bonding. For the fabrication of double-gate devices, the SiO_2 layer which covers the emitters at this step is left as protection from ambient air and particles.

C. FIB assisted collimation gate aperture fabrication

In the final steps, we fabricate G_{col}. On the FEA chip with the patterned G_{ext}, we deposit a 1.2 μm thick SiON second insulation layer (I_2) by PECVD, followed by a 500 nm thick sputtered Mo layer (G_{col}). The PECVD conditions of the SiON deposition were optimized to reduce the residual stress of the film well below 0.1 GPa. The BOE etching rate of the SiON of I_2 used here is three times slower than that of the SiO_2 of I_1. This difference in etching rates is important to prevent over-etching of I_2 in the last BOE etching step (Fig. 3(d)), necessary to remove the SiON and SiO_2 layers, and to expose the emitter tips.

To minimize the emission current reduction at finite V_{col}, we require the G_{col} apertures to be approximately three times larger than the G_{ext} apertures.[9] This is difficult to achieve in a reproducible way by the self-aligned etch-back process used for G_{ext} because the required diameter is larger than the protrusions on top of the emitter tips obtained after the deposition of the I_2 and G_{col} layers. Therefore, we developed a method using FIB milling with Ga ions (FEI Strata DB 235). We found that the direct milling through the G_{col} electrode makes the underlying SiON layer inert to BOE, perhaps due to Ga ion implantation in the SiON layer. Hence, we add two sacrificial layers (750 nm of SiO_2 and 100 nm of Mo) and use them as mask for the G_{col} etching [Fig. 3(a)]. Using the FIB, we mill through the two sacrificial layers and about one half of the G_{col} layer [Fig. 3(b)]. The remainder of G_{col} is removed by wet-etching afterwards, using the patterned sacrificial SiO_2 layer as the etching mask. The topmost Mo layer, which is needed to avoid charging of the chip surface during the FIB milling, is removed during the wet-etching of G_{col} at the same time [Fig. 3(c)]. The FIB milling time was approximately 90 s per aperture with 6 μm diameter using an ion current of 1.5 nA. This amounts to a total FIB milling time for the 20×20 tip array of approximately 10 h without including the time required for stage movements and drift correction.

Using the patterned gate apertures as mask, we then wet-etch the insulation layers (I_1, I_2) in BOE as depicted in Fig. 3(d). As mentioned above, the undercut in I_2 at this step is minimized owing to the slower SiON etch rate compared to SiO_2. About ~0.5 μm of the I_1 layer thickness is left unetched to minimize the exposure of the emitter tip apexes to ambient air. It is etched off just before inserting the FEA into the experimental chamber. In Fig. 4(a), we show a top-

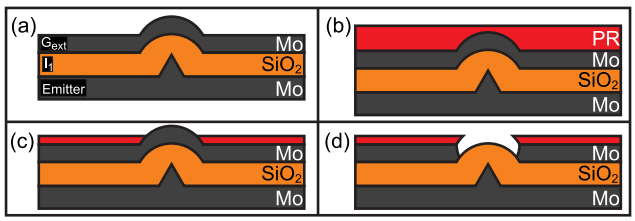

FIG. 2. The process steps applied to fabricate the electron extraction gate electrode by the polymer etch-back method. (a) Deposition of the insulator I_1 and the extraction gate electrode G_{ext} layers. (b) Spin-coating of a PR layer. (c) Oxygen plasma etching of the PR until the metal on top of the emitters is laid bare. (d) Use the patterned PR as wet-etching mask for the extraction gate apertures.

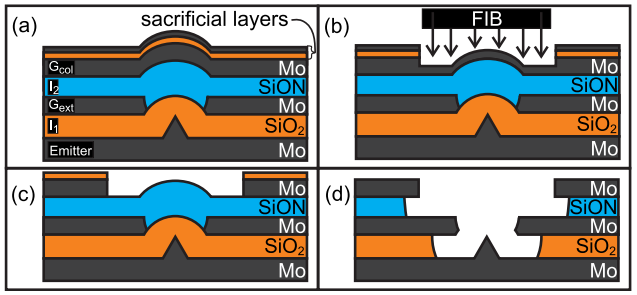

FIG. 3. Process steps to fabricate the collimation gate (G_{col}) by the FIB assisted method. (a) After the fabrication of the G_{ext} aperture, the insulator I_2, the G_{col} layer and the sacrificial layers (SiO_2 (lower), and Mo (upper) are deposited. (b) FIB milling through the sacrificial layers and one half of the G_{col} layer. (c) The G_{col} aperture is finalized by wet-etching. This step also removes the sacrificial Mo layer. (d) BOE etching to remove I_1 and I_2 on top of the emitters using G_{ext} and G_{col} as etching masks. This step also removes the sacrificial SiO_2 layer.

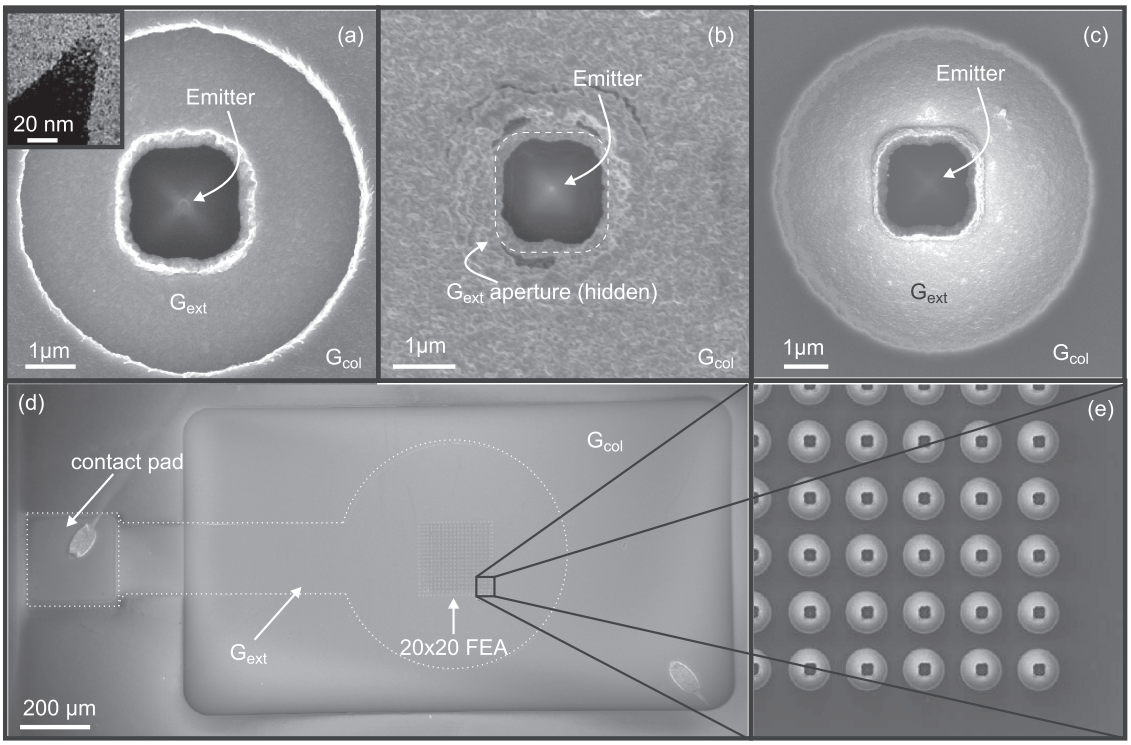

FIG. 4. Top-view SEM micrographs of double-gate FEAs. (a) FEA1 (one of the emitters) with a TEM cross-section of the tip apex (inset). (b) FEA2 (one of the emitters). The dotted line approximately shows the underlying G_{ext} aperture. (c) FEA3 (one of the emitters). (d) Overview of FEA3. The 20×20 emitters are located at the center of the rectangular G_{col} electrode with a size of 2.5×0.75 mm. The G_{ext} electrode is a 500 μm diameter circle with a 0.04 mm^2 rectangular contact pad attached at the end (partially buried underneath G_{col} as indicated by the dotted lines). The oxide on top of the 0.2 mm square contact pad at the end is etched away before the wire bonding.

view SEM image of FEA1 with a G_{ext} diameter of 2.3 ± 0.1 μm and a G_{col} diameter of 6.2 ± 0.1 μm. High-resolution transmission electron microscopy (TEM) imaging of an emitter on the same FEA substrate as FEA1 (inset of Fig. 4(a)) shows that the emitter apex radius of curvature is ~7.5 nm.

Next, the G_{col} electrode of each array is patterned into a rectangular shape of approximately 2.5 mm × 0.75 mm with rounded corners as shown in Fig. 4(d) for FEA3. The G_{ext} electrode is buried underneath G_{col}. G_{ext} is electrically contacted through the 0.2 mm square via etched into I_2 on top of the G_{ext} contact pad. The comparatively large G_{col} aperture (Fig. 4(a) for FEA1 and Fig. 4(c) for FEA3, and in contrast, Fig. 4(b) for FEA2) provides electro-static shielding of the emitted electrons from the G_{ext} potential or non-uniform electric fields created by the bonding wires and prevents beam distortions. The electrical contact to G_{col} is made by bonding wires to one corner of G_{col} [Fig. 4(d)].

III. EXPERIMENTAL SETUP AND SAMPLE PREPARATION PROCEDURE

A. Field emission microscope

The field emission current-voltage characteristics measurement and the beam imaging were conducted in a field emission microscope schematically shown in Fig. 5. We imaged the electron beam on a metalized P43 phosphor screen after amplifying it with a micro-channel plate (MCP) inserted between the FEA and the phosphor screen. The distance between the MCP front plate and the FEA can be adjusted by a linear translation mechanism and was typically set to 40–50 mm. The electron beam was accelerated by applying a DC potential of 1 kV to the front-plate of the MCP which also functions as the anode in this setup. To amplify the beam, we applied 1.7 kV to the back-plate of the MCP leading to an amplification factor of ~10^3. The

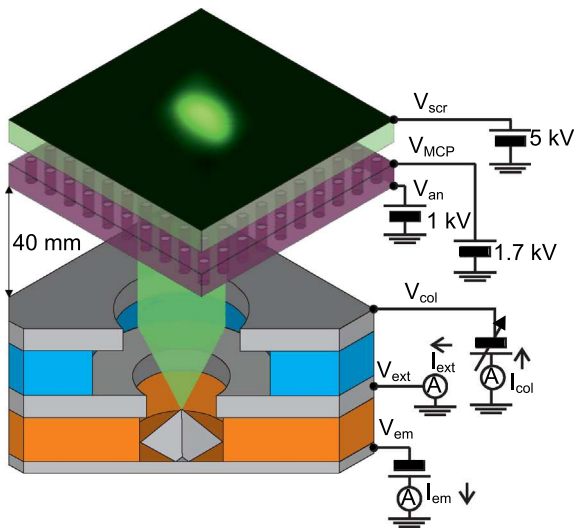

FIG. 5. Schematic diagram of the field emission microscope. The field emission electron beam is amplified by a micro-channel plate biased by (V_{MCP}-V_{an}) and imaged by the phosphor screen (biased at a voltage V_{scr} of 3-5 kV). The currents I_{em}, I_{ext}, and I_{col} were recorded simultaneously while controlling the bias voltages V_{em} and V_{col}. V_{ext} is normally fixed to ground potential.

phosphor screen was biased at 5 kV. A full-color video recorder with 8-bit resolution per color (Canon XL1s) was used to record the phosphor screen images of FEA1 and FEA2. Auto-brightness adjustment was turned off during the experiment to allow for the calculation of the current density from the image brightness. The FEA3 beam images were recorded by a full HD Sony Handycam. The brightness of the images was adjusted by the shutter time, which was kept constant during the whole experiment.

The captured images were subsequently analyzed to evaluate the beam size and the current density. The beam size was extracted by the automatic pattern recognition algorithm described in the supplementary materials.[38]

The FEA chip was mounted on a ceramic (MACOR) holder. To be able to load up to three double-gate FEAs at the same time, we prepared 6 contact terminals for gate electrodes and 1 terminal to be connected with the emitter substrate (via a copper plate underneath the FEA chip) on the holder. These were connected to BNC electrical feedthroughs using Kapton insulated wires. The FEA gate electrodes were wire-bonded by 25 μm thick aluminum wires to Au-plated ceramic bonding pads fixed on the sample holder.

To generate a collimated field emission beam, a negative electron extraction potential V_{em} was applied to the emitter substrate with respect to G_{ext}, thereby initiating electron field emission from the tips. A negative beam collimation potential V_{col} was applied to G_{col} with respect to G_{ext}. G_{ext} was set to ground potential. The current I_{em} injected into the emitter substrate, the G_{ext} current I_{ext}, and the G_{col} current I_{col} were simultaneously measured. The net emission current I_{net} that reached the screen was evaluated by $(|I_{\mathrm{em}}| - I_{\mathrm{ext}} - I_{\mathrm{col}})$. For the FEA3 experiment, it was possible to measure I_{net} directly by inserting a coaxial Faraday cup in front of the FEA chip.

B. FEA preparation procedure

After the BOE etching removal of the remaining SiO_2 layer on top of the emitter tips and wire-bonding to the gate contacts, we quickly loaded the FEA into the field emission microscope chamber and evacuated it with a turbo-molecular pump for 24–48 h while heating the chamber to 140 °C. After this baking, we switched from the turbo-molecular pump to an ion getter pump. The final base pressure was $\sim 5 \times 10^{-9}$ mbar.

At the beginning of the experiment, the field emission current was erratic and fluctuated over several orders of magnitude. It became stable after a conditioning process, in which the FEAs were operated for a prolonged time period. We scanned V_{em} slowly with G_{col} and G_{ext} connected to ground potential while measuring the currents I_{em}, I_{ext}, and I_{col}. V_{em} was scanned between zero volts and a negative maximum with a period of 2–10 cycles/min. For the 2×2 arrays (FEA1 and FEA2), I_{net} was indirectly measured via I_{em}, I_{ext}, and I_{col}. I_{net} of the 20×20 array (FEA3) was directly measured by the Faraday cup. During the initial conditioning phase, the scan range of V_{em} was slowly increased over the course of several days while observing the stability and the increase of the emission current. A more stable and higher emission current is normally obtained by this conditioning. This is likely due to desorption of remaining adsorbents on the tip surface initiated by the emitted current, e.g., via Joule heating. Gentle increase of the scan range of V_{em} may also have helped rounding off atomic protrusions by Joule heating without causing arcs, but the detailed mechanism has not been established yet.[37] After the current-voltage characteristics had stabilized by conditioning, we started the beam imaging experiment.

IV. RESULTS AND DISCUSSIONS

A. The influence of the G_{col} aperture size on the beam collimation characteristics

In Figs. 6(a), 6(c), and 6(e), we present the experimental results of FEA1 with G_{ext} and G_{col} aperture diameters of $2.3 \pm 0.1\ \mu$m and $6.2 \pm 0.1\ \mu$m, respectively.[9] Fig. 6(a) shows a set of three phosphor screen images of FEA1 after the conditioning. The images were taken at different V_{col} of +1 V, −31 V, and −61 V from left to right. V_{em} was fixed at −80 V. I_{net} was equal to 0.5–1 nA for these three images. V_{em} and therefore I_{net} were kept low to avoid destructive arcing. The FEA-MCP separation was 40 mm. Reduction of the beam size and simultaneous increase of the beam brightness with the decrease of V_{col} are apparent.

The increased beam brightness indicates a minimal decrease of the emission current with the decrease of the beam size. In fact, as the current-voltage characteristics in Fig. 6(c) show, I_{net} was approximately 0.5 ± 0.2 nA for V_{col} in the range from +1 V to −65 V. The gate currents I_{col} and I_{ext} were less than 20% of I_{net} in the same V_{col} range. As summarized in Fig. 6(e), the average beam radius R_{s} was reduced from 7.2 ± 0.4 mm ($V_{col} = +1$ V) to 1.0 ± 0.2 mm ($V_{col} = -69$ V). Here, we defined R_{s} as the radius of the circle which encloses 80% of the beam area. Combining this with the observed I_{net}, we found that the current density was increased by a factor of 13.9 ± 1.0. When V_{col} was lower than −69 V or, differently put, the ratio k_{col} of V_{col} to V_{em} larger than 0.86, I_{net} fell to zero. We ascribe this to the repulsion of the extracted electrons by the G_{col} potential and their subsequent collection by G_{ext}. This interpretation is consistent with the observation that I_{ext} increased for k_{col} above 0.86 [Fig. 6(c)].[25–30]

We note that, since the acceleration potential V_{an} applied to the MCP front plate is an order of magnitude larger than V_{em}, R_s is proportional to the rms transverse velocity $u_{\|}$. The relation is given by

$$\frac{R_s}{2\sqrt{2\ln|0.2|}L_s} = \frac{u_{\|}}{u_{an}}\left(\sqrt{1+\frac{u_0^2}{u_{an}^2}} - \frac{u_0}{u_{an}}\right), \qquad (1)$$

where L_{s} is the FEA-MCP separation and the velocity u_{an} is given by $\sqrt{2qV_{an}/m}$ (with q the elementary charge and m the electron rest mass). In Eq. (1), we defined the initial longitudinal velocity u_0 as the electron velocity at 1–10 μm off the emitter apex. Even though the classical electron velocity at the emitter apex surface is zero, u_0 is finite because the finite V_{em} accelerates the electrons. For the uncollimated beam at $V_{col} = 0$, u_0 is to a good approximation given by

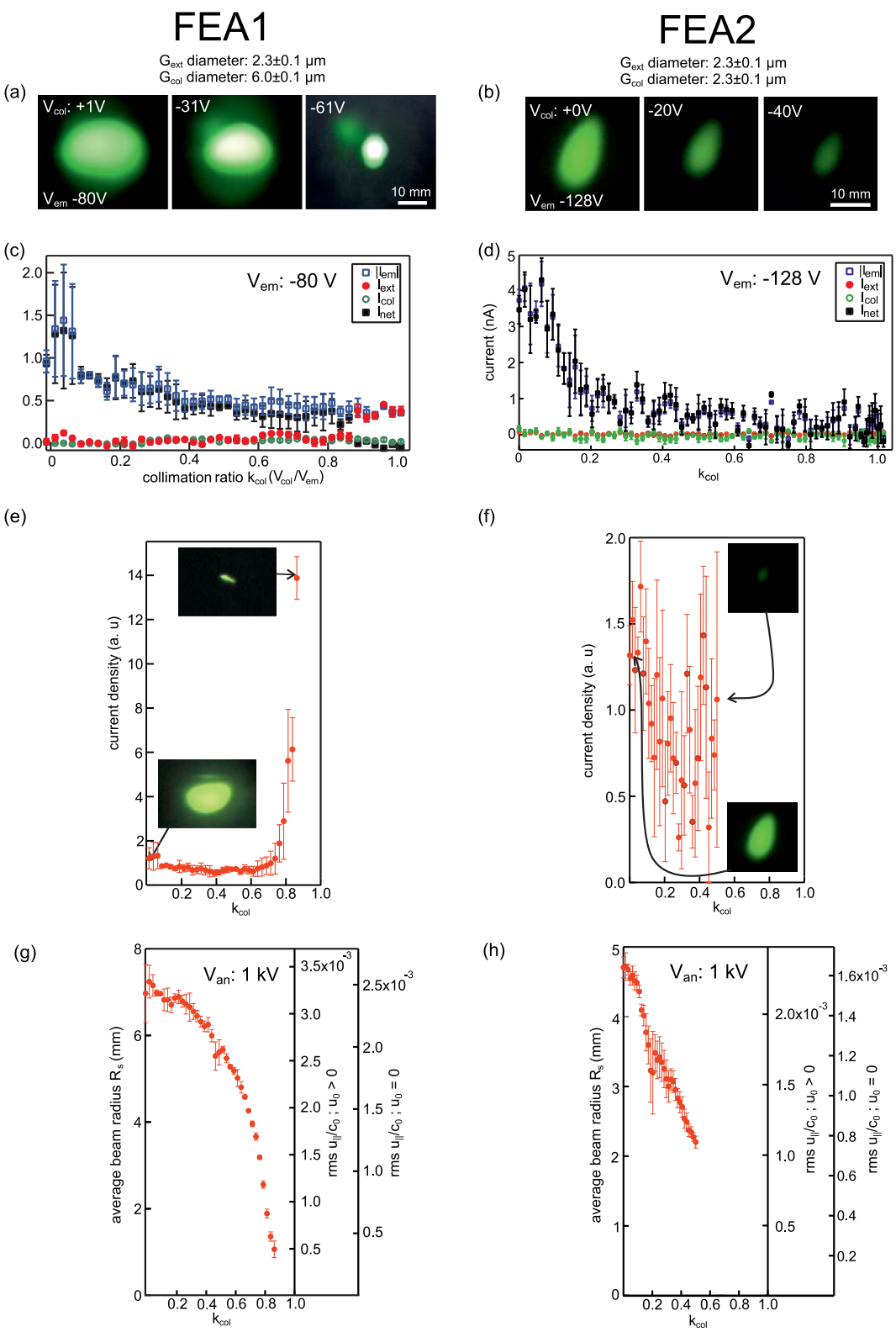

FIG. 6. Summary of the field emission characteristics of FEA1 (G_{col} aperture diameter of $6.2 \pm 0.1\,\mu$m, left panel) and FEA2 (G_{col} aperture diameter of $2.3 \pm 0.1\,\mu$m, right panel) measured with the acceleration voltage V_{an} set to 1 kV. (a) FEA1 beam images with V_{col} of +1 V, −31 V, and −61 V. V_{em} was fixed at −80 V. (b) FEA2 beam images with V_{col} of 0, −20, and −40 V. V_{em} was fixed at −128 V. (c) and (d) The current-voltage characteristics of FEA1 and FEA2, where open squares depict the emitter current I_{em}, solid squares the net current I_{net}, filled circles the extraction gate current I_{ext}, and open circles represent the collimation gate current I_{col}. The horizontal axis depicts the ratio k_{col} of V_{col} to V_{em}, where V_{em} was −80 V for FEA1 and −128 V for FEA2, respectively. (e) The relation between the current density and k_{col} of FEA1 (V_{em} of −80 V). The two inset images show the beam at k_{col} of 0 (bottom) and 0.86 (top). (f) The relation between the current density and k_{col} of FEA2 (V_{em} of −128 V). The two inset images show the FEA2 beam at a k_{col} of 0 (bottom) and 0.5 (top). (g) and (h) The relation between the average beam radius R_s (left axis) and k_{col} with $V_{an} = 1$ kV for FEA1 (g, with $V_{em} = -80$ V) and FEA2 (h, with $V_{em} = -128$ V). The right axes show the rms transverse electron velocity evaluated from R_s for the two case $u_0 = 0$ (outermost right axis) and $u_0 > 0$ (inner right axis).

$\sqrt{2q|V_{em}|/m}$ and $u_{||}$ is of the same order of magnitude as u_0. For the collimated beam with V_{col} close to V_{em}, the G_{col} potential decelerates the electrons and u_0 and $u_{||}$ become substantially smaller. Thus, we can safely assume u_0 equal to zero for the evaluation of $u_{||}$ of the maximally collimated beam which makes it insensitive to the actual value of u_0. Additional assumptions to relate R_s and $u_{||}$ by Eq. (1) are discussed in the supplementary material.[38]

In Fig. 6(g), we summarized R_s as a function of k_{col}. The two right vertical axes of Fig. 6(g) indicate the evaluated $u_{||}$ from Eq. (1) for two cases: (i) u_0 equal to $\sqrt{2q|V_{em}|/m}$ and (ii) zero u_0. We found that $u_{||}$ is equal to 3.3×10^{-3} c_0 at zero k_{col} and equal to 3.7×10^{-4} c_0 at the maximum k_{col} of 0.86, where c_0 is the speed of light in vacuum. From these values, we found that $u_{||}$ was reduced by a factor of 8.9 at k_{col} of 0.86.

To experimentally investigate the impact of the large G_{col} aperture of FEA1 on the strong beam collimation, we compare the beam characteristics of FEA1 with FEA2. The most important difference of FEA2 is its small G_{col} aperture diameter of 2.3 ± 0.1 μm, which is approximately equal to the G_{ext} aperture diameter of 2.3 ± 0.1 μm. Figs. 6(b), 6(d), 6(f), and 6(h) summarize the experimental results of FEA2. As shown in Fig. 6(d), the emission current decreased rapidly with the increase of k_{col}. We note that the maximum V_{em} was set to -128 V for FEA2 to increase the emission current and to make the beam image observable at large k_{col}. Nevertheless, the emission current became negligible at k_{col} beyond 0.3. This is in stark contrast to the behavior of FEA1 but similar to the previously reported double-gate FEAs with small G_{col} aperture diameters fabricated by the resist etch-back method.[24] The beam size (and $u_{||}$) decreased (Figs. 6(b) and 6(h)) with the increase of k_{col}. As a consequence of the rapid decrease of the emission current with k_{col}, however, no enhancement of the beam brightness and current density were observed (Figs. 6(b) and 6(f)). We also repeated the same measurements at lower V_{em} values to rule out the possibility that the large V_{em} (-128 V) influenced the results but the behavior was unchanged. The value of $k_{col} > 0.3$ for which I_{em} fell below 10% of its value at $k_{col} = 0$ was also found to be independent of V_{em}.

B. Emission characteristics of a 20×20 double-gate FEA

To test the fabrication method and the collimation characteristics of a FEA with a larger number of emitter tips, we fabricated a 20×20 emitter array (FEA3) [see Figs. 4(c) and 4(e)]. The top-view SEM image in Fig. 4(c) shows a magnified view of one of the emitters of FEA3. FEA3 has G_{ext} aperture diameters of 2.0 ± 0.1 μm and G_{col} aperture diameters of 7.2 ± 0.1 μm. These values are similar to the gate aperture diameters of FEA1. As shown in Fig. 7, the I_{net}-k_{col} relation of FEA3 was similar to that of FEA1. When V_{em} was equal to -60 V, I_{net} decreased monotonously with the increase of k_{col}. I_{ext} started to increase at a k_{col} of 0.95 and reached 50% of I_{em} at a k_{col} of 0.99.

As shown in Figs. 8(a) and 8(b), R_s decreased from $\sim$3.8 mm to $\sim$0.45 mm when k_{col} was increased from 0 to 0.98 (measured at V_{em} of -82 V). As shown in Figs. 8(c) and 8(d), I_{net} at the largest V_{em} decreased from 280 nA to 40 nA with the increase of k_{col} from 0 to 0.98. I_{ext} was negligible at k_{col} of 0 but increased to $\sim$25% of I_{em} at k_{col} of 0.98. Hence, we conclude that the major cause of the I_{net} decrease with the increase of k_{col} is due to the reduction of F_{tip} with the increase of the collimation potential. Combining R_s with the observed I_{net}, we found that the current density enhancement at $k_{col} = 0.98$ was equal to $\sim$13.7.

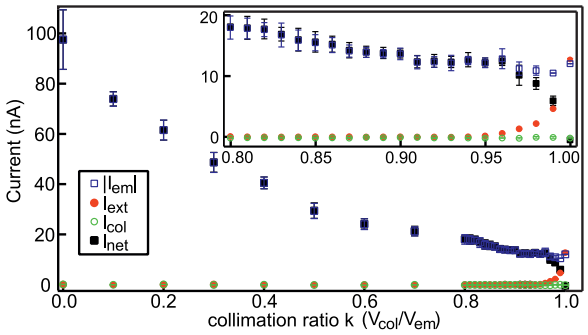

FIG. 7. Current-voltage characteristics of the 20×20 emitter array FEA3. Emitter current I_{em} (open squares), net current I_{net} (solid squares), extraction gate current I_{ext} (filled circles), and the collimation gate current I_{col} (open circles) at various ratios k_{col} ($=V_{col}/V_{em}$) at a V_{em} of -60 V. The inset shows a close up view of the same data for k_{col} between 0.8 and 1.0.

We also evaluated $u_{||}$ at these k_{col} values using Eq. (1). We found $u_{||}$ equal to 2.7×10^{-3} c_0 at $k_{col} = 0$ (with u_0 determined by V_{em} of -82 V) and 2.4×10^{-4} c_0 at $k_{col} = 0.98$ (assuming $u_0 \sim 0$). Therefore, $u_{||}$ was reduced by a factor of $\sim$11.3. This reduction is $\sim$27% higher than in the case of FEA1. Furthermore, the smallest $u_{||}$ of FEA3 at k_{col} equal to 0.98 is 1.9 times smaller than the smallest $u_{||}$ of FEA1 at k_{col} equal to 0.86 (at the maximum current density condition).

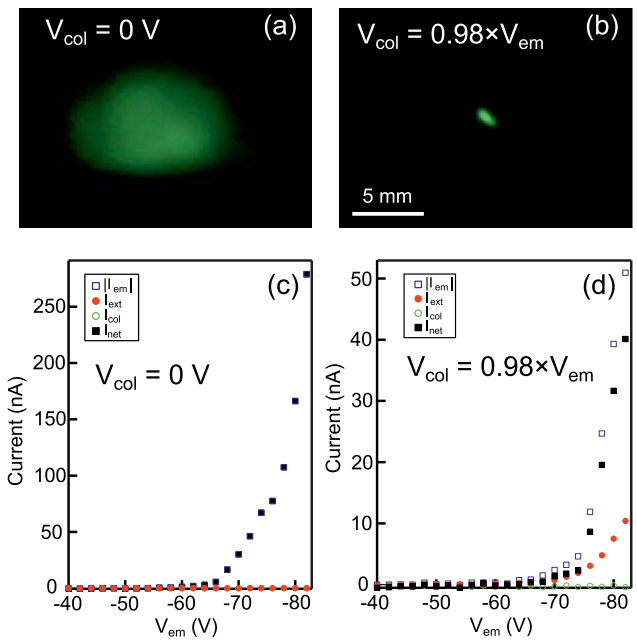

FIG. 8. Beam images of the 20×20 emitter array FEA3 recorded at k_{col} ($=V_{col}/V_{em}$) equal to 0 (a) and k_{col} equal to 0.98 (b); V_{em} was -82 V and the corresponding I_{net} equal to 280 nA in (a) and 40 nA in (b), respectively. (c) and (d) The I-V characteristics of the full V_{em} scan. The images in (a) and (b) were recorded at the maximum V_{em} of (c) and (d), respectively.

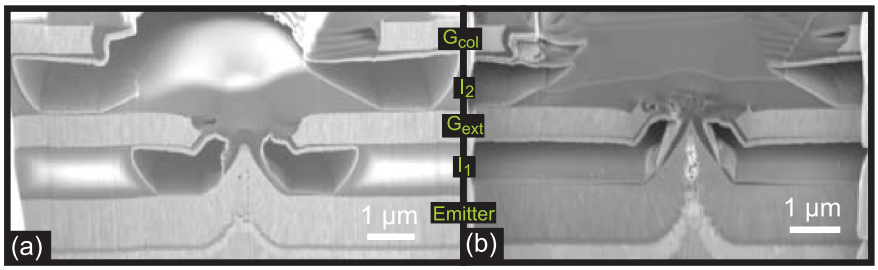

FIG. 9. FIB cross-sections of one of the emitters of (a) FEA1 and (b) FEA3. The comparison of the G_{ext} aperture edge shapes shows that FEA3 has a $\sim$0.2 μm tall collar blocking the direct line of sight from the emitter tip to G_{col}. No such collar can be found at the G_{ext} edge of FEA1.

We assume that these differences between FEA1 and FEA3 originate from the small difference in the gate aperture shapes as suggested by the top-view SEM images in Fig. 4. To investigate this in detail, we prepared cross-sections of one of the emitters from each of the two FEAs using FIB milling (Fig. 9). The various layers are indicated in the middle of the figure. (The dark carbon layer visible mainly around the tip and G_{ext} was deposited prior to the FIB milling to avoid the collapse of the gate layers.) The comparison of the cross-sections of the two FEAs revealed a $\sim$0.2 μm tall collar at the G_{ext} edge of FEA3, which is absent for FEA1. This is a consequence of the slightly shorter mask etching and wet-etching times for the G_{ext} aperture patterning of FEA3. The height of the collar is consistent with the top-view SEM images which show a $\sim$0.2 μm smaller inscribed diameter of G_{ext} of FEA3 compared to that of FEA1 (Figs. 4(a) and 4(c)). Although the height of the collar is less than $\sim$10% of the G_{ext} diameter, combined with the $\sim$1 μm larger G_{col} aperture diameter, an extra shielding of the emitter apex from G_{col} was introduced, preventing a direct line of sight from the emitter tip apex to G_{col}. Neo *et al.* demonstrated the effectiveness of such shielding recently with volcano-shaped double-gate FEAs (Refs. 28 and 29). We expect even higher current densities and lower rms transverse velocities with double-gate FEAs with a higher G_{ext} collar providing better electro-static shielding of the emitter tip.

V. SUMMARY AND CONCLUSIONS

We presented the fabrication method and the electron beam characteristics of double-gate FEAs with G_{col} aperture diameters approximately three times the size of the G_{ext} apertures and showed that these devices can generate a highly collimated field emission beam with enhanced current density. The comparison of the field emission characteristics of FEA1 and FEA3 with large G_{col} apertures with FEA2 with small G_{col} apertures showed that the large difference in G_{ext} and G_{col} aperture diameter is necessary to achieve significant enhancement of the current density. The scalability of the high-brightness emission current was demonstrated by the successful fabrication and the beam characteristics measurements of the 20×20 emitter array device. In addition, a detailed comparison of the beam characteristics and the gate structures between FEA1 and FEA3 indicated that further improvement of the beam collimation can be achieved by optimizing the G_{ext} aperture. The planar G_{col} surface of our FEAs is likely to be advantageous for the operation in high acceleration electric fields of 10 MV/m and above[10,11] by reducing the probability of parasitic emission from the top surface and subsequent vacuum breakdown.

These results were achieved by the developed FIB assisted G_{col} fabrication method, which we found to be more reliable and stable than the self-aligned resist etch-back method. Yet, the 20×20 tip array appears to be the practical limit in up-scaling the array size because of the required milling time of the available FIB tool. Nevertheless, the capabilities of the FIB such as its flexibility and the mask-less patterning are certainly attractive for studying various device structures with a small number of emitter tips.

We note that although the emission current of the 20×20 FEA was proportionally higher than that of the 2×2 FEA, further increase of the average current to above 4 μA per tip is expected from our FEAs as demonstrated for single-gate FEAs with 20×20 tip arrays[5] and 10^4 tip arrays.[12] With the 10^4 tip array, this has been achieved with the help of a noble gas conditioning process which can also improve the beam uniformity. The proposed mechanism assumes impact ionization of noble gas molecules close to the current emitting tips and subsequent ion bombardment of these tips. Therefore, we can potentially accelerate the emission homogenization process in double-gate FEAs by applying a positive bias to G_{col} while the FEA is in a noble gas atmosphere. Such noble gas conditioning experiments on double-gate FEAs are currently being conducted.

A detailed comparison of the beam characteristics with the FIB cross-sections of FEA1 and FEA3 indicates the possibility of further performance improvement. Particularly interesting is the fact that we were able to increase k_{col} to 0.98 for FEA3, thereby obtaining a higher maximum current density and smaller transverse velocity than with FEA1. How far k_{col} can be increased in a given device seems to be highly sensitive to the detailed structure of the gate aperture openings and emitter tip apexes. Another important question is the impact of the G_{col} aperture shape and the inhomogeneity of the alignment of G_{col} with the tip (better than $\sim$0.2 μm precision in the current process) on the emission current quenching at large k_{col}. To investigate these questions and elucidate the performance limitation of double-gate FEAs, further experimental explorations of the device structure and the operation conditions in combination with numerical simulations, which takes into account the actual tip shape and the gate structures, are necessary.

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